Curriculum Vitae

Peter Jeremy Wilson

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Summary

An experienced innovator and computer architect, specializing in the embedded space with demonstrated capability to both create and to synthesize concepts and apply them to improving a product; to demonstrate through modeling and simulation the value of the changes - including the construction of novel tools as needed - and to assess and propose appropriate changes to the software toolchain to make use of the innovations, including the proposal and demonstration of new language features. My communication skills allow me to communicate the rationale, details and value of the changes to management and customers.

My broad work history demonstrates a pattern of innovation leading to commercial success: it includes the initiation of RapidIO; the definition of the PowerPC Book E architecture; the creation of the e200 family of synthesizable PowerPC cores, giving access to a ~$2B lifetime TAM; the architecture of the Freescale e500 PowerPC processor including the DSP-oriented SPE extensions; the VLE extensions to PowerPC architecture which added $100M to e200 lifetime TAM; the creation of a concurrent extension to C/C++ and of an Architecture Description Language now deployed within Freescale, a leading semiconductor company.
most recently

Most recently, I initiated and drove the quarq Architecture Research Project in Freescale/NXP's Discovery Labs. The project defined a highly efficient embedded-friendly architecture which deployed many (from one to hundreds or thousands) multicontext processor cores, low-cost inter-context message-passing through a wormhole mesh network, and a static homing cache coherent memory. We collaborated with the internal Freescale compiler team to get an llvm compiler built. We exercised the architecture in simulation across a wide range of application domains including network packet processing, file compression and expansion, vision systems based on Histograms of Oriented Gradients (HoG) and most recently in collaboration with Professor Omer Khan and his students at U. Connecticut in Convolutional Neural Networks.

As a result of the purchase of Freescale by NXP, I retired from NXP in December 2016.

Professional Experience

Kiva Design Groupe LLC, Leander, Texas

CTO, 1994 - present

Kiva Design Groupe is a small company acting as a vehicle to support consultancy and contractual works.

Consultancy activities in the past included:

- Mining through active patents for processor/systems-related IP of possible business interest for Freescale, including the construction of simple software to ease the search through plain-text versions of the patents.

- Providing technical skills in defending allegations of IP infringement for Freescale
- Driving inventions through the patent/invention disclosure process at Freescale
- Architecture, simulation advice and work for Spansion, who was building flash-memory-oriented SoCs
- Design and implementation of low-level boot code and embedded flash firmware drivers for one such SoC
- Collaborating on multicore software directions and technologies with PolyCore, a software startup
- Became an LLC in February 2017

NXP/Freescale Semiconductor, Austin, Texas

quarq Architecture Research Project Leader, FDL, 2013-2016

Freescale created the Freescale Discovery Labs to support longer-term investigation and discovery than was usually possible in product-introduction-centric business units. I was instrumental in triggering the creation of the Labs, and had my proposal for an architecture research project accepted early.

The quarq architecture addressed the apparent need for a power-efficient, scalable, general purpose processor. The basis was that systems were constructed form one to many (hundreds or thousands) of cores. Each core could communicate with others using a mesh communications network (we simulated a wormhole-routed 2-D mesh), using architected user-mode instructions which could send a message to a destination, or await a message on a port. The cores supported multiple contexts, and context-swapped automatically on a priority basis. We collaborated with the FSL compiler team, and triggered the import of llvm compiler technology into the company. The architecture was novel in the sense that it selected and combined known science into a useful piece of engineering.

We used the compiler to construct a number of applications, including network packet processing, compression and decompression of files, simple DSP, vision processing with HoG, and finally convolutional neural networks. We found the architecture to scale well, to offer significantly higher performance per sq mm of silicon than GPUs, and to be straightforward to program.

We defined the architecture using ADL, which generated an executable model, assembler, and disassembler for us; the compiler generated assembler output.

We collaborated with Professor Omer Khan of U. Connecticut, who contributed effort to the porting of a version of the MIT Graphite system model (to provide accurate modeling of memory system and communications performance) and to the creation, tuning and analysis of the CNN work.

Intellectual Property Licensing Department, 2008-2013

Freescale's IPL department provides substantial low-overhead revenues to the company through the licensing of the company's intellectual property portfolio, consisting of several thousand patents. In addition, the technical experts in the department often provide technical assistance to the Law Department in defensive matters, and provide technical briefings and support to external counsel in both offensive and defensive lawsuits.

- Supported external counsel for defensive matters in Freescale's successful ITC lawsuit against Panasonic in 2010
- Supported external counsel for offensive matters in Freescale's successful ITC lawsuit against Panasonic in 2010
- Mined for assertable patents
- Provided defensive technical advice for multiple "troll" attacks against Freescale

- Wrote software to allow useful queries against a text-only version of the Freescale patent portfolio, including the beginnings of a concurrent version in Google's Go language.

Technology Office, NCSG Advanced Technology Division (ATD), 2004 - 2006

ATD was created both to provide new processor core designs and to explore, select, prototype and provide for integration advanced technologies relevant to the business of the Networking and Computing Systems Group. The Technology Office concentrated on future needs, my emphasis being on the issues of multicore designs and the management of the architectural explosion likely to result from multicore systems.

- Defined Plasma, a concurrent extension to C/C++ for systems and software modeling and real time distributed software implementation
- Drove pilot implementation of Plasma
- Drove and collaborated on the design of Freescale ADL, an Architecture Design Language allowing layered representation of a computer architecture and the automatic construction of a range of tools including documentation, a verification ISS, a time-approximate execution-driven performance model, assembler, etc. ADL is now in production use within Freescale and has been open-sourced.
- Drove initial implementation of ADL
- Initiated and collaborated in the investigation of microADL, a language for describing processor pipelines and allowing the automatic construction of clock-accurate execution-driven performance models as well as of compiler back-ends when combined with an ADL specification
- Commenced investigation of lightweight concurrency architecture suitable for multicore embedded systems, and of prototype compiler construction
- Proposed an adaptive compiler for microarchitecture investigation (the pipeline under investigation being defined in a text file), collaborated with external vendor, and drove contract for such a compiler-in-the-loop for use with a new synthesizable e200 core
- Customer involvement in the automotive space, explaining future systems directions and gathering feedback

Distinguished Member of Technical Staff, 2002 - 2004

As senior individual contributor, initially drove aspects of SPS-wide IP management, IP acquisition and IP cataloguing. Transitioned to the e200 team, which defined and implemented a family of synthesizable PowerPC cores. Led and drove architecture issues, verification ISS creation, product strategy and customer relations.

- Handled architecture investigation and tool construction for reduced code footprint ISA extensions for PowerPC
- Definition, project management of the collaboration with our compiler team and analysis of VLE, the deployed reduced code footprint extensions for PowerPC. The introduction of VLE to the e200 increased lifetime automotive TAM by several $100M
- Developed concept and prototype for e200 architecture description language, followed by driving e200 implementation of the language and tool allowing automatic construction of a verification ISS now used in production functional verification of e200s and which acted as a proof of existence and basis for the Freescale ADL

Thoughtbeam, Inc., a Motorola Company, Austin, Texas

Manager, Advanced Systems Architecture and Distinguished Member of Technical Staff, 2001 - 2002

Joined Thoughtbeam (which was an internal Motorola start up) at its inception. Thoughtbeam was formed to commercialize what was believed to be breakthrough technology capable of growing high quality III-V semiconductor films - such as Gallium Arsenide- on silicon substrates, allowing the integration of logic and optical subsystems and the construction of very high speed logic.

- Hired-in because of history of innovation
- Filed more than 12 disclosures on systems applications of the technology
- Defined product roadmap, concentrating on communications/networking and high-performance processing
- Active role in the recruitment of staff and executives
- Ranked and rated internal disclosures, choosing what inventions got filed

Motorola Semiconductor Products Sector, Austin, Texas

Architecture and System Platforms/Somerset Design Center

Member of Technical Staff, 1997 - 2001

Somerset was the name given to the joint Apple/IBM/Motorola Design Center founded to commercialize new PowerPC architecture. Somerset became Motorola-only in 1998.

- Represented Motorola on the tripartite PowerPC Architecture Committee
- Crafted aspects of the Book E contract between IBM and Motorola defining an embedded oriented improvement to the PowerPC ISA
- Represented Motorola in the definition of the Book E architecture and drove aspects of the architecture including simplified MMU and improved interrupt architecture
- Initiated the design of high-speed point-to-point systems interconnect (commercialized later as RapidIO) supporting directory based cache coherence
- Drove the creation of over 30 disclosures on aspects of RapidIO, including two of my own inventions
- Investigated the fit between PowerPC and hard realtime embedded automotive applications, culminating in the definition of the e500 core with novel RTOS in silicon, DSP-oriented SIMD and other innovations
- Represented Motorola in technical due diligence exercises when acquisitions and partnerships were mooted, including C-Port
- Initiated the creation of the e200 family of synthesizable PowerPC cores, defining the goals and preferred implementation of the first core immediately before and overlapping with time at Thoughtbeam. This core family now (2007) forms the heart of the eSys family of automotive products, representing a lifetime TAM of around $2,000,000,000 and without which Freescale/SPS could well have lost its dominance in this marketplace

Bull HN, Austin, Texas

Director, Microsystems Architecture, 1992 - 1997

Bull HN is the U.S. arm of Groupe Bull, a multinational computer company (whose major shareholders at the time were the French State, NEC and Motorola); its revenues approximated $6,000,000,000 worldwide. In 1991, Bull decided that its current UNIX line, based on MIPS processors, was not adequate for its future needs, and embarked on a search for a replacement. Oversaw processor related aspects of the eventual partnership with IBM for PowerPC.

- Assessed the PowerPC 620 system bus architecture
- Researched into architecture and software needs of distributed next generation "PDA" system
- Designed and implemented a new generation of software tools providing a simple capability-based OS and language suitable for both next generation PDA systems and simulation
- Created novel MP verification tools, one a little language describing the state machine in the 620 BIU to allow automatic construction of verification tests and the other an automatic generator of self-checking parallel programs for use in verification
- Drove technical aspects of partnership with Motorola Computer Group resulting in MCG becoming first OEM customer for Bull's MP PowerPC systems and later resulting in Motorola becoming a Bull shareholder
- Performed research into latency-surviving memory mechanisms
- Appointed Bull Fellow when this position was introduced.

Bull HN, Billerica, Massachusetts

Director, Design Validation, 1990 - 1992

This position at Bull was created as the company was beginning its move away from mainframes into the distributed and client/server UNIX world. In embracing a move as large as this, the VP, Systems Engineering saw the need for a small group to experiment with the future through simulation, prototyping and subcontracting to improve the likelihood that choices made would work well. Later played a part in assessing which RISC architecture and which company Bull should partner with as it drove to expand its UNIX business.

- Managed and directed a small group - three professionals plus two students
- Managed contracts with an outside consultancy investigating and prototyping an accelerated RPC implementation
- Defined and constructed a new simulation language leveraging *csp* concepts
- Analyzed the performance of MIPS R4000 processor on TPC-C-like workloads using the simulation language, in partnership with an outside company developing out-of-order speculative execution microprocessors
- Constructed a massively-parallel free-text format search engine prototype
- Analyzed the needs of next generation wireless PDAs.
- Performed technical due diligence assessing PowerPC, DEC Alpha and HP architectures and systems offerings

N Systems, Colorado Springs, Colorado

Chief Scientist, 1989 - 1990

N Systems was a self-funded start up to be funded by venture capital. Its business plan foresaw a profitable business being a one-stop shop for UNIX workstation designs - a licensee was to be able to obtain a hardware design (N-Systems-designed ASICs) for a high performance, low cost SPARCStation workalike together with a UNIX port plus support all from one source.

- Defined a simulation language
- Implemented the language, leveraging C macros and a discrete-event simulation engine
- Performed initial modeling of the workstation design

Prisma Inc., Colorado Springs, Colorado

System Architect, 1987 - 1989

Prisma was a start up, venture-funded, established in 1986 with seed-round funding in early 1987. Its original business plan was to use the experience of its founders in very high speed Gallium Arsenide technology to build a remarkably compact real time supercomputer offering scalar performance exceeding a typical Cray in the confines of a cubic foot or so, but the investors drove the company toward the construction of yet another Unix hot box. As a result of a number of unfortunate circumstances, its Board chose to close Prisma in November 1989.

- Drove technical aspects of choice between MIPS, SPARC and proprietary architectures, including discussions with the two companies.
- Designed and implemented a discrete event simulation package to perform microarchitectural investigations
- Designed and implemented an execution-driven microarchitecture model using the simulation package
- Defined the system microarchitecture out to the memory and the I/O subsystem
- Developed a strong team through interviewing and hiring
- Conceived of and oversaw the construction of an automated verification test suite generator
- Provided liaison between the hardware and software teams

INMOS Corporation, Colorado Springs, Colorado

Microcomputer Applications Manager, 1983 - 1987

INMOS (now a fragment of SGS-Thomson) was a semiconductor company established simultaneously in the UK and the U.S.A. with the intention of being suppliers of market-leading high performance memories and microprocessors. The microprocessor was the transputer, and its architecture was focused on parallel programming; however, its very novelty and its unique programming language - *occam* - meant that marketing the family in the U.S. required significant in-depth understanding of the machine, its applications and the rationale behind its design choices together with the communication skills - verbal and written - to impart the information to customers; having been part of the transputer architecture team in the UK end of INMOS, I was asked by the President/CEO to relocate to the U.S. to head the technical half of the marketing team behind the transputer family in the U.S.

- Built a technical applications team

- Appeared at trade shows, wrote articles in trade magazines and made customer visits touting and explaining architecture and products
- Provided consultancy to major customers
- Created a consultants network to help support the product
- Drove and supported third-party compiler vendors
- Created the network of FAEs

INMOS Ltd., Bristol, England

Engineer, 1979 - 1983

Prior to relocating to the U.S., worked with the transputer group in Bristol in a number of positions. Initially I joined the group responsible for investigating the possibilities for the transputer family, with specific responsibilities for interprocessor communications.

- Performed ISA analysis and design
- Drove the investigation into and analysis of the construction of intelligent peripherals (disk/file controller and graphics controller) integrating transputer processor and logic
- Spurred the creation of the INMOS G170 Color Look-Up Table device later adopted by IBM for the VGA standard
- Preformed pre-launch technical marketing activities including creating, making and giving confidential presentations to commercial, university and government audiences.

International Computers Ltd., Kidsgrove, England

Engineer, 1974 - 1979

ICL was the IBM of England, albeit on a smaller scale. I worked for a group whose responsibilities were for various communications systems and subsystems, and worked both in Scotland and in the English Midlands when the group relocated there.

- Design Authority for all 7502-based products
- Investigated and implemented new architecture capabilities in the 7502 family making use of exceptions, reducing code footprint by 30% with concomitant reduction in deployed system cost
- Appointed a member of the Microprocessor Standards Committee, reviewing and recommending actions associated with new microprocessors
- Performed technical due-diligence investigation of external partners

Ferranti Ltd., Bracknell, England

Engineer, 1969 - 1974

Ferranti was an engineering company; their Digital Systems Division in Bracknell specialized in providing real time computer systems to the British Navy.

- Owned, developed, implemented, instrumented and tuned a real time adaptive tracking package for military targets sensed by surveillance radar
- Managed the team implementing the radar pattern-recognition software

- Appointed as a Future Software Committee member
- Defined components of an architecture for a small-domain capability-based distributed hard real time architecture and RTOS, and prototyping of the RTOS
- Collaborated with the F100L team, implementing a very early 16 bit microprocessor

Granted Patents

US4601031: Repairable ROM Array (joint with CPH Walker)

US5293424: Secure Memory Card (joint with T Holtey)

US5896517: High performance processor employing background memory move mechanism

US6032207: Search mechanism for a queue system

US6472694: Microprocessor structure having a compound semiconductor layer (joint with M Pandya)

US6754752: Multiple memory coherence groups in a single system and method therefore (joint with B Marietta)

US8402327B2:Memory system with error correction and method of operation (joint with Perry Pelley and George Hoekstra)

US8990546B2: Data processing system with safe call and return

US9507654B2: Data processing system having messaging

US9092647B2: Programmable Direct Memory Access Channels (joint with Joseph C. Circello, Daniel M. McCarthy, John D. Mitchell, John J. Vaglica)

US8861243B1: Four port memory with multiple cores (joint with Perry Pelley)

Published Patent Applications

US20060155974: Data processing system having flexible instruction capability and selection mechanism (joint with W Moyer)

US20140282564A1 Thread-suspending execution Barrier (with Eli Almog and Michele W. Adkins)

US20130138930A1: Computer Systems and methods for register-based message-passing

US14321957: Systems and Methods for Processing Inline Constants (joint with Brian Kahne and Jeffrey Scott)

US20150046658A1: Cache organization and method

US14667229: Computer systems and methods for context switching (joint with Brian Kahne)

US20160342421A: Computer systems and methods for executing contexts with autonomous functional units (joint with Brian Kahne)

Education

Sheffield University, BSc Physics and Pure Maths, England, 1969.

Abingdon (Roysse's) School, education to A and S levels.

Publications and Appearances

- To appear at IPDPS 2017 - paper on CNNs on quarqs "Accelerating Graph and Machine Learning Workloads Using a Shared Memory Multicore Architecture with Auxiliary Support for in-Hardware Explicit Messaging"

- Halit Dogan, Farrukh Hijaz, Masab Ahmad, Omer Khan - U. of Connecticut, Storrs, CT, USA
- Brian Kahne, Peter Wilson, - NXP Semiconductors, Austin, TX, USA

- "An Introduction to the Plasma Language," Brian Kahne, Aseem Gupta, Peter Wilson, Nikil Dutt; Microprocessor Test and Verification Conference, Austin 2005.
- "Architecture, Embedded Systems, and the Future," Vail IEEE Computer Elements Workshop, June 2005.
- "Optimizing Your PowerPC Device Software: Tips and Tricks," Tomas Evensen, Wind River and Pete Wilson. Announcement of VLE and a discussion of future architecture trends and their impact on toolchains.
- Translation of "Serveurs Multiprocesseurs, Clusters, et Architectures Paralleles," Rene J Chevance, 2000 with collaboration on content and additional material, into "Server Architectures," Rene J Chevance, Elsevier Digital Press 20005. ISBN 1-55558-333-4.
- A variety of trade magazine articles and industry conference appearances, including:
  - IEEE Vail 2005 Computer Workshop;
  - Invited keynote speaker at inaugural Cool Chips, Tokyo (1997),
  - Panel session at Hot Chips (What I'd do If I Were Designing Merced) (1998);
  - a joint paper on 620 MP verification techniques at the 1995 IPCCC (related papers at other symposia);
  - three papers at IEEE Asilomar Microcomputer Workshop (on how to destroy a start up; the architectural needs of PDAs; and a critique of PowerPC).
  - a number of articles for Byte magazine won 'Best in issue' awards (90's),
  - a paper at Hot Chips on the Prisma P1 GaAs embedded supercomputer architecture;
  - many articles in the computer press and at trade conference on transputers and occam.

Personal

Member, ACM and Life Member IEEE. Enjoy travel, especially with a camera - once 35mm, now digital. High fidelity sound reproduction.